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DATE MAILED: 09/04/2002

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO	
09/842,768	04/27/2001	Yu Zhu	0020-4855P	2830	
2292	7590 09/04/2002				
BIRCH STEWART KOLASCH & BIRCH			EXAMINER		
PO BOX 74 FALLS CH	7 JRCH, VA 22040-074	7	JONES, STEPHEN E		
			ART UNIT	PAPER NUMBER	
			2817		

Please find below and/or attached an Office communication concerning this application or proceeding.

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	Application No.	Applicant(s)	•••				
	09/842,768	ZHU ET AL.					
Office Action Summary	Examiner	Art Unit					
	Stephen E. Jones	2817	<u></u>				
The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply							
A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication. - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely. - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication. - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). - Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b). Status							
1) Responsive to communication(s) filed on	<u> </u>						
2a)☐ This action is FINAL . 2b)⊠ Th	is action is non-final.						
3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under <i>Ex.parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213. Disposition of Claims							
4) Claim(s) 1-7 is/are pending in the application.							
4a) Of the above claim(s) is/are withdrawn from consideration.							
5) Claim(s) is/are allowed.							
6)⊠ Claim(s) <u>1-7</u> is/are rejected.							
7) Claim(s) is/are objected to.	,						
8) Claim(s) are subject to restriction and/or election requirement.							
Application Papers							
9) The specification is objected to by the Examiner.							
10)☐ The drawing(s) filed on is/are: a)☐ accepted or b)☐ objected to by the Examiner.							
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).							
11) The proposed drawing correction filed on is: a) approved b) disapproved by the Examiner.							
If approved, corrected drawings are required in reply to this Office action.							
12) The oath or declaration is objected to by the Examiner.							
Priority under 35 U.S.C. §§ 119 and 120							
13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).							
a)⊠ All b)☐ Some * c)☐ None of:							
1. Certified copies of the priority documents have been received.							
2. Certified copies of the priority documents have been received in Application No.							
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the certified copies not received.							
14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).							
a) ☐ The translation of the foreign language provisional application has been received. 15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.							
Attachment(s)							
1) Notice of References Cited (PTO-892) 2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) Information Disclosure Statement(s) (PTO-1449) Paper No(s) 5	5) Notice of Informal	y (PTO-413) Paper No(s Patent Application (PTO					

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DETAILED ACTION

Claim Objections

1. Claims 1, 2, 4, and 6 are objected to because of the following informalities:

It appears that the term "plane" should read as --planar-- to describe the planar nature of the "impedance matching circuit".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

- 2. The following is a quotation of the second paragraph of 35 U.S.C. 112:
 - The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.
- 3. Claims 4-5 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding Claim 4, it is not clear what the phrase "at the other end thereof" is referring, thus rendering the claim vague and indefinite.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

5. Claims 1-3 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Eda et al.

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Eda et al. (Fig. 5) discloses a high frequency circuit including: a plurality layers; a via hole (224) penetrating the layers; a planar impedance matching circuit (221) is connected to a signal line (201, 225) and the via for matching the impedance of the signal line (Claims 1 and 2). Regarding claim 3, note that the phrase "by adjusting a width and a length" is not given any patentable weight, especially since the final product does not appear to actually be adjustable (i.e. only the final product is patentable in an apparatus claim, and it appears that applicant's "adjusting step" is merely pre-selecting the length and width to affect the impedance).

6. Claims 1-3 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Yoshikawa et al.

Yoshikawa et al. (Figs. 2, 3a-c) discloses a high frequency circuit including: a plurality layers; a via hole penetrating the layers; a planar impedance matching circuit (8) is connected to a signal line and the via for matching the impedance of the signal line (Claims 1 and 2). Regarding claim 3, note that the phrase "by adjusting a width and a length" is not given any patentable weight, especially since the final product does not appear to actually be adjustable (i.e. only the final product is patentable in an apparatus claim, and it appears that applicant's "adjusting step" is merely pre-selecting the length and width to affect the impedance).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

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(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

- 8. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).
- 9. Claims 4-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eda et al.

Eda et al. teaches a circuit as described above. Eda et al. also teaches connecting a stub to the impedance matching line (221) (see Col. 8, lines 15-19) for impedance matching.

However, Eda et al. does not explicitly teach using one stub on each side of the matching line (Claim 4).

It would have been considered obvious to one of ordinary skill in the art to have modified the Eda et al. matching line to have included one stub on each side of the matching line instead of the single stub taught by Eda, because it would have allowed

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for a mere optimization of the impedance matching determined by the pre-selected signal line's impedance, thereby suggesting the obviousness of such a modification.

Regarding Claim 5, note that the phrase "by adjusting a width and a length" is not given any patentable weight (see the rejection of claim 3 above for details).

10. Claims 4-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshikawa et al.

Yoshikawa et al. teaches a circuit as described above. Yoshikawa et al. also teaches connecting a stub to the impedance matching line (e.g. see Col. 3, lines 30-35) for impedance matching.

However, Yoshikawa et al. does not explicitly teach using one stub on each side of the matching line.

It would have been considered obvious to one of ordinary skill in the art to have modified the Yoshikawa et al. matching line to have included one stub on each side of the matching line instead of the single stub taught by Yoshikawa, because it would have allowed for a mere optimization of the impedance matching determined by the preselected signal line's impedance, thereby suggesting the obviousness of such a modification.

Regarding Claim 5, note that the phrase "by adjusting a width and a length" is not given any patentable weight (see the rejection of claim 3 above for details).

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11. Claims 6-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eda et al. in view of Okada et al. (US 5,701,128).

Eda et al. teaches a circuit as described above. However, Eda et al. does not teach that the impedance matching line and stub are formed of a plurality of series lines of different widths.

Okada et al. (Figs. 21-23 and Col. 7, lines 65-678 to Col. 8, lines 1-3) teaches that stubs connected to transmission lines are an equivalent impedance matching circuit method to lines having different widths connected in series.

It would have been considered obvious to one of ordinary skill in the art to have substituted a matching line having varying widths such as taught by Okada et al. in place of the matching stub circuit in the Eda structure, because it would have provided an art-recognized functionally equivalent impedance matching means, thereby suggesting the obviousness of such a modification.

Regarding Claim 7, note that the phrase "by adjusting a width and a length" is not given any patentable weight (see the rejection of claim 3 above for details).

12. Claims 6-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshikawa et al. in view of Okada et al. (US 5,701,128).

Yoshikawa et al. teaches a circuit as described above. However, Yoshikawa et al. does not teach that the impedance matching line and stub are formed of a plurality of series lines of different widths.

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Okada et al. (Figs. 21-23 and Col. 7, lines 65-678 to Col. 8, lines 1-3) teaches that stubs connected to transmission lines are an equivalent impedance matching circuit method to lines having different widths connected in series.

It would have been considered obvious to one of ordinary skill in the art to have substituted a matching line having varying widths such as taught by Okada et al. in place of the matching stub circuit in the Yoshikawa structure, because it would have provided an art-recognized functionally equivalent impedance matching means.

Regarding Claim 7, note that the phrase "by adjusting a width and a length" is not given any patentable weight (see the rejection of claim 3 above for details).

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Miyauchi et al. teaches an integrated circuit device.

Lampen et al. teaches a direct backside interconnect.

Okada et al. (5,525,953) teaches a multi-plate cable.

Josefsson et al. teaches an impedance matching stripline transition.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen E. Jones whose telephone number is 703-305-0390. The examiner can normally be reached on Monday through Friday from 8 AM to 4 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert J. Pascal can be reached on 703-308-4909. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-6251 for regular communications and 703-308-6251 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-

0956.

BENNY T. LEE PRIMARY EXAMINER ART UNIT 2817

SEJ

August 30, 2002